UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,799	12/22/2000	Zhengwei Zhang	TI-31654	4577

23494 7590 01/31/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
JERABEK, KELLY L	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 01/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,799	ZHANG ET AL.	
	Examiner	Art Unit	
	Kelly L. Jerabek	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24 and 25* is/are allowed.

6)☒ Claim(s) *1-3,6,7,10-13,15 and 18-21* is/are rejected.

7)☒ Claim(s) *4,5,8,9,14,16,17,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of the second species pertaining to claims 1-25 in the reply filed on 9/23/2004 is acknowledged.

Drawings

Figures 9 and 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6-7, 10-13 and 18-21 rejected under 35 U.S.C. 102(b) as being anticipated by the applicants conceded prior art.

Re claim 1, the applicants conceded prior art discloses in figure 9 a CMOS imaging sensor including a pixel block, a column block, and a chip output block. Figure 10 summarizes the positions of the switches (SEL, RES, CDS, COL, CHIP) during the integration period and pixel readout, which enables the fixed pattern noise to be suppressed. The pixel block of figure 9 is a pixel circuit for sensing image information. The column block and the chip output block serve as a readout circuit for reading out the image information. Readout steps 1-5 are described in the applicant's specification (pages 3-4). Capacitor (C1) is switched into and out of connection between a variety of different pairs of nodes depending on whether the switches (SEL, RES, CDS, COL, CHIP) are opened or closed. Figure 10 discloses whether the switches are open or closed for each of the readout steps (steps 1-5). Therefore, the capacitor is switched into and out of connection between each of first and second pairs of nodes of the

readout circuit. For example, at readout step 2 the capacitor is connected between a first pair of nodes corresponding to the SEL switch being closed and the CDS switch being closed; and at readout step 3 the capacitor is connected between a second pair of nodes corresponding to the SEL switch being closed and the CDS switch being open.

Re claim 2, at readout step 2 the SEL switch is closed and the CDS switch is closed. The examiner is reading the nodes on each end of the capacitor during readout step 2 as the first pair of nodes. The voltage across C1 becomes VPD-VN1gs (specification: page 3, lines 8-10). When the Sequential Correlated Double Sampling Technique is performed VN1gs and VP1gs are canceled and the fixed pattern noise is greatly reduced (specification: page 4, lines 3-6). Therefore, the capacitor (C1) stores charge (VN1gs) for reducing noise when it is connected between the first pair of nodes corresponding to the SEL switch being closed and the CDS switch being closed during readout step 2.

Re claim 3, the noise includes fixed pattern noise (specification: page 4, lines 3-6).

Re claim 6, at readout step 2 the SEL switch is closed and the CDS switch is closed. The examiner is reading the nodes on each end of the capacitor during readout step 2 as the first pair of nodes. The voltage across C1 becomes VPD-VN1gs (specification: page 3, lines 8-10). Since all of the steps 1-5 are readout steps, the

examiner is reading the readout step 2 (corresponding to the SEL switch being closed and the CDS switch being closed) as a step for reading out image information.

Re claim 7, the applicant's admitted prior art states that at readout step 3 the SEL switch is closed and the CDS switch is open. The examiner is reading the nodes on each end of the capacitor during readout step 3 as the second pair of nodes. The voltage across C1 remains VPD-VN1gs (specification: page 3, lines 11-12). When the Sequential Correlated Double Sampling Technique is performed VN1gs and VP1gs are canceled and the fixed pattern noise is greatly reduced (specification: page 4, lines 3-6). Therefore, the capacitor (C1) stores charge (VN1gs) for reducing noise when it is connected between the second pair of nodes corresponding to the SEL switch being closed and the CDS switch being open during readout step 3.

Re claim 10, the image sensor of figure 9 is a CMOS image sensor and the capacitors are poly/n-well capacitors (specification: page 4, lines 13-17).

Re claim 11, the applicant's admitted prior art includes a capacitor (C1) that is switched into and out of connection between a variety of different pairs of nodes depending on whether the switches (SEL, RES, CDS, COL, CHIP) are opened or closed. Figure 10 discloses whether the switches are open or closed for each of the readout steps (steps 1-5). Therefore, the capacitor is switched into and out of connection between each of first and second pairs of nodes of the readout circuit. The

examiner is reading the switching arrangement of readout step 1 as the capacitor being connected between a first pair of nodes corresponding to the SEL switch being closed and the CDS switch being closed; and the examiner is reading the switching arrangement of readout step 3 as the capacitor being connected between a second pair of nodes corresponding to the SEL switch being closed and the CDS switch being open. The switching arrangements of the SEL and CDS switches are opposite for readout steps 1 and 3, therefore it can be seen that the first node of the first pair is electrically distinct from the first nod of the second pair and the second node of the first pair is electrically distinct from the second node of the second pair. Since the CMOS imaging device includes a capacitor and a switching arrangement it is inherent that the capacitor includes a first capacitor plate for connection to a first node of each of the pairs and a second capacitor plate for connection to a second node of each of the pairs.

Re claim 12, see claim 11.

Re claim 13, see claim 11.

Re claim 18, see claim 1.

Re claim 19, see claim 2.

Re claim 20, at readout step 3 the SEL switch is closed and the CDS switch is open. The examiner is reading the nodes on each end of the capacitor during readout step 3 as the second pair of nodes. The voltage across C1 remains VPD-VN1gs (specification: page 3, lines 11-12). Since all of the steps 1-5 are readout steps, the examiner is reading the readout step 3 (corresponding to the SEL switch being closed and the CDS switch being open) as a step for reading out image information.

Re claim 21, at readout step 2 the SEL switch is closed and the CDS switch is closed. The examiner is reading the nodes on each end of the capacitor during readout step 2 as the first pair of nodes. The voltage across C1 becomes VPD-VN1gs (specification: page 3, lines 8-10). Since all of the steps 1-5 are readout steps, the examiner is reading the readout step 2 (corresponding to the SEL switch being closed and the CDS switch being closed) as a step for reading out image information.

Claims 1 and 15 rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. US 6,128,039.

Re claim 1, Chen discloses in figure 2 a column of active pixel cells (301) for sensing image information. The active pixel cells (301) are input to a readout circuit (column amplifier (305)) for reading out the image information (col. 3, lines 56-67). The column amplifier (305) includes a sense capacitor (C1), an operational amplifier (307), a feedback capacitor (C2), an output capacitor (C3), an output buffer (311), and switches

S1, S2, S3 (col. 4, lines 1-8). Figure 5 shows a series of timing diagrams for the switches. At time (t1) the switch (S1) is closed thus allowing the image signal level Vimg to be stored on the capacitor (C1)(col. 5, lines 3-19). The examiner is reading the timing (t1) as switching the capacitor (C1) into connection between a first pair of nodes. At time (t2) the control signal for switch (S1) transitions low and switch (S1) opens. The image signal level Vimg remains stored on the capacitor (C1) (col. 5, lines 20-25). The examiner is reading the timing (t2) as switching the capacitor (C1) into connection between a second pair of nodes. Therefore, it can be seen that the switching arrangement disclosed by Chen switches the capacitor (C1) into and out of connection between each of first and second pairs of nodes of the readout circuit.

Re claim 15, the readout circuit (305) disclosed by Chen includes a buffer (311) having an input coupled to the switching arrangement for connection to the pixel circuit (301) and an output for outputting the image information of the readout circuit (fig. 2; col. 4, lines 20-29).

Allowable Subject Matter

Claims 4-5, 8-9, 14, 16-17, and 22-23 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fail to anticipate or render obvious the following technical features as recited in the highlighted claims:

Re claims 4-5, 8-9, 14, 17, and 22-23, the prior art fails to teach or suggest that one of the nodes of the switching arrangement is a low impedance node.

Re claim 16, the prior art fails to teach or suggest "...wherein said buffer output is one of said nodes of said first pair and said buffer input is one of said nodes of said second pair".

Claims 24 and 25 allowed.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fail to anticipate or render obvious the following technical features as recited in the highlighted claims:

Re claims 24-25, the prior art fails to teach or suggest "A method of controlling an image sensor apparatus including...switching a capacitor into a first configuration having connection between the second supply voltage and the output of the buffer; and then switching the capacitor into a second configuration having connection between the output of a pixel circuit and the input of the buffer, such that the capacitor, when the

capacitor is in the first configuration a compensating voltage is stored therein including components incidental to the readout of the pixel voltage, and when the capacitor is in the second configuration the incidental voltage components are cancelled".

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chen et al. (US 6,248,991) discloses a sequential correlated double sampling technique for CMOS area array sensors. The information regarding a switched capacitor arrangement for reducing fixed pattern noise is relevant material.

Chen et al. (US 6697108) discloses fast frame readout architecture for array sensors with an integrated correlated double sampling system. The information regarding a switched capacitor arrangement for reducing fixed pattern noise is relevant material.

Sauer (US 6,320,616) discloses a CMOS image sensor with reduced fixed pattern noise. The information regarding a switched capacitor arrangement for reducing fixed pattern noise is relevant material.

Badyal (US 5,534,815) discloses a switching circuit for signal sampling with reduced residual charge effects. The information regarding a switched capacitor arrangement is relevant material.

Tomasini et al. (US 5,978,025) discloses an adaptive optical sensor. The information regarding a switched capacitor arrangement is relevant material.

Kozlowski et al. (US 6,535,247) discloses an active pixel sensor with capacitorless correlated double sampling. The information regarding using correlated double sampling to reduce noise is relevant material.

Fossum et al. (US 6,665,013) discloses an active pixel sensor having intra-pixel charge transfer with an analog-to-digital converter. The information regarding a switched capacitor arrangement is relevant material.

Okamoto et al. (US 6,423,958) discloses a solid state imaging device and method of driving the same. The information regarding a switched capacitor arrangement is relevant material.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on **(571) 272-7308**. The fax phone number for submitting all Official communications is 703-872-9306. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at **(571) 273-7312**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLJ

TUAN HO
PRIMARY EXAMINER